Executive Summary – Michael Ashford

Contributions

FPGA Design

- Libero installation and troubleshooting
- Initial FPGA testing and setup
- Research RISC-V, find viable options
- Research programming
- Design initial prototype
- Write C code to run on CPU
- Research and pick out code for benchmark tests
- Create new RISC-V configurations for comparison testing

PCB Design

- Find a suitable LCD Screen and Paddle Switch
- Import and create footprints and CAD models
- Create schematics linking LCD Screen and Switch to FMC
- Route traces for final PCB layout

Final Report

- Write Executive Summary
- Create documentation for FPGA Configurations
- Create documentation for Benchmark Testing
- Work on final presentation
- Gather Libero Projects together and upload

Time Table

Week #	**Hours spent**	**Work done**
1	5	Researched Triple Modular Redundancy
2	5	Learning VHDL coding Researching TMR and LCDs
3	7	Learning VHDL coding Researching TMR and LCDs
4	8	Get acquainted with Libero Build modules for LCD screen Integrate LCD into Altium Build RISC-V Processor
5	12	Build RISC-V Processor Build PWM Module Find a paddle switch
6	15	Reinstall Libero Build RISC-V Processor Build LCD Interface
7	8	Fix Libero with help of Tech Support Setup Git in Libero
8	14	Build RISC-V Processor Build LCD Altium Schematic Integrate Paddle Switch into Altium Created initial code for LCD in SoftConsole
9	9	Put RISC-V Core in TMR PCB trace routing
10	13	Routed PCB Program LCD Implement extra external device communication
11	13	Routed PCB Program LCD Research benchmarking
12	10	Configure FP version of RISC-V core Work on documentation Benchmarking
13	20	Create new RISC-V Configurations Work on final documentation Work on oral presentation Benchmarking SoftConsole Code Commenting
Total Hours:	149	