## Executive Summary – Michael Ashford

## Contributions

FPGA Design

- Libero installation and troubleshooting
- Initial FPGA testing and setup
- Research RISC-V, find viable options
- Research programming
- Design initial prototype
- Write C code to run on CPU
- Research and pick out code for benchmark tests
- Create new RISC-V configurations for comparison testing

PCB Design

- Find a suitable LCD Screen and Paddle Switch
- Import and create footprints and CAD models
- Create schematics linking LCD Screen and Switch to FMC
- Route traces for final PCB layout

Final Report

- Write Executive Summary
- Create documentation for FPGA Configurations
- Create documentation for Benchmark Testing
- Work on final presentation
- Gather Libero Projects together and upload

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1     5     Researched Triple Modular Redundancy       2     5     Learning VHDL coding Researching TMR and LCDs       3     7     Learning VHDL coding Researching TMR and LCDs       4     8     Get acquainted with Libero Build modules for LCD screen Integrate LCD into Altium Build RISC-V Processor       5     12     Build RISC-V Processor Build PWM Module       6     15     Reinstall Libero Build LCD Interface       7     8     Fix Libero with help of Tech Support Setup Git in Libero Build LCD Interface       8     14     Build RISC-V Processor Build LCD Interface       8     14     Build RISC-V Processor Build LCD Altium Schematic Integrate Paddle Switch into Altium Created initial code for LCD in SoftConsole       9     9     Put RISC-V Core in TMR PCB trace routing       10     13     Routed PCB Program LCD Research benchmarking       12     10     Configure FP version of RISC-V core Work on documentation Benchmarking       13     20     Create new RISC-V Configurations	Week #	Hours spent	Work done
Researching TMR and LCDs7Learning VHDL coding Researching TMR and LCDs48Get acquainted with Libero Build modules for LCD screen Integrate LCD into Altium Build RISC-V Processor512Build RISC-V Processor Build PVMM Module Find a paddle switch615Reinstall Libero Build RISC-V Processor Build LISC-V Core in TMR PCB trace routing99Put RISC-V Core in TMR PCB trace routing1013Routed PCB Program LCD Research benchmarking1113Routed PCB Program LCD Research benchmarking1210Configure FP version of RISC-V core Work on documentation Benchmarking1320Create new RISC-V Configurations	1	5	Researched Triple Modular Redundancy
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13 20 Create new RISC-V Configurations			Work on documentation
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Work on final documentation	13	20	Create new RISC-V Configurations
work on final documentation			Work on final documentation
Work on oral presentation			Work on oral presentation
Benchmarking			Benchmarking
SoftConsole Code Commenting			SoftConsole Code Commenting
Total 149	Total	149	
Hours:	Hours:		