Proposal

Triple Modular Redundancy Implemented Through RISC-V Architecture on an FPGA

PO# PC11801312

by

BYU-Idaho ECEN 499 W20 Senior Design Team

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Team members:

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Description:

Create and test a system using Triple Modular Redundancy (TMR) with various configurations of the RISC-V open source instruction set on Microsemi's PolarFire radiation tolerant FPGA. This is to test the possibility of using RISC-V architecture in space, specifically the possibility of implementing this system in the Caution and Warning System (CWS) in the xEMU.

Methodology:

Altium will be used to design the PCB to breakout peripherals and include components that are listed in the hardware section of the document. The finished PCB design will be sent out to a company to print, and we will manually populate and solder the components.

To implement the TMR RISC-V cores, and program the PolarFire board, Microsemi's IDE will be used to create the VHDL code. Due to only having one license for this, Xilinx's Vivado will be used, along with Digilent's Basys3 board, will be used to design and test the communication hardware where possible and then transferred to the PolarFire once completed.

Hardware:

- PolarFire FPGA by Microsemi
- LCD Screen
- Radiation Sensor (Geiger Counter)
- Heartrate Monitor
- Pressure Sensor
- Temperature/Humidity Sensor

- Custom PCB with headers for GPIO, SPI, I2C, and UART. Ordered from China
- LEDs, switches, buzzers

Our custom PCB will house the LCD, the various sensors and components in use, and the connector that will attach onto the FPGA. We wanted to focus on monitoring astronaut vitals while in their suits. The heartrate monitor will look out for any elevations that could indicate problems. The temperature and humidity sensor will be used for temperature control in the suit. The pressure sensor will look out for suit leaks. The radiation sensor will monitor outside conditions and alert the astronaut to critical amounts of radiation. LEDs and buzzers will supplement the LCD screen in alerting the astronaut to danger.

Deliverables:

First deliverable will be this proposal. Afterwards, there will be a weekly status update on the project. At the end of the project, there will be the source code and documentation for the project, report on all research and testing done, JSC Form 290, completed PCB, and the PolarFire FPGA flashed with the final system design.

Schedule:

Task	People Assigned	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	WK10	WK11	WK12	WK13
		12-Jan-20	19-Jan-20	26-Jan-20	2-Feb-20	9-Feb-20	16-Feb-20	23-Feb-20	1-Mar-20	8-Mar-20	15-Mar-20	22-Mar-20	29-Mar-20	6-Apr-20
		Sun	Sun	Sun	Sun	Sun	Sun	Sun	Sun	Sun	Sun	Sun	Sun	Thu
PCB														
Design Multi-Channel ADC Circuit	Max			.	.	.	.							
LEDs (some RGB), Switches, GPIO Headers	James			.	.	.								
SPI & I2C Ports	James			.	.	.								
Radiation Sensor, Temperature and Humidity Sensor	Zac			.	.	.								
Heartrate Sensor, Pressure Sensor	Sam			.	.	.	.							
LCD Screen Interface (like the NHD-C0216CZ-FSW-FBW-3v3)	Michael			.	.	.								
UART Connector (50 pin)	James			.	.	.								
Design PCB Layout	Max, Sam, James					.	.	.	.					
Assemble PCB	Max, Sam, James								.	.	.			
COMM														
10 Full-DuplexUART (Using Hamming Code and FIFOs)	James		.				.	.	.	.				
SPI	Max		.	.	.	.	.							
I2C	Sam					.	.	.						
PWM	Zac					.	.	.						
TMR/CPU														
Implement RISC-V cores with varying configurations	Michael, Zac				.	.	.	.	.					
RISC-V TMR	Michael, Zac					.	.	.	.	.				
FRAM TMR	Michael, Zac					.	.	.	.	.				
TESTING														
Write code to test system & peripherals	ALL									.	.	.	.	
Run Standard CPU Benchmarks	ALL							.	.	.	.	.		
Determine Ideal RISC-V Configuration	ALL											.	.	
DELIVERIES														
Poster														.
Demonstration & Oral Report														.
Final Report													.	.