NASA
TMR RISC-V MCU for CWS

ECEN 499

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Overview:

- **Purpose**
- **Goals**
- **Hardware & Software**
- **Libero**
- **SoftConsole**
- **Altium**
- **Future Areas of Improvement**

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Purpose:

Using the PolarFire FPGA Eval kit and a custom PCB, benchmark various RISC-V core configurations in Triple Modular Redundancy (TMR) for use in NASA's Caution and Warning System (CWS) in the Portable Life Support System (PLSS) of the newest space suit (xEMU).

Goals:

- PCB
  - Multi-Channel ADC
  - LEDs, Switches, GPIO Headers
  - Accelerometer, Temperature and Humidity Sensor
  - Heartrate Sensor, Pressure Sensor
  - LCD Screen, FMC connector
- Communication
  - 10 Full-Duplex UART
  - SPI
  - I2C
  - PWM
- Create multiple configurations of RISC-V cores in TMR
- Benchmark configurations and create a detailed report of the outcome

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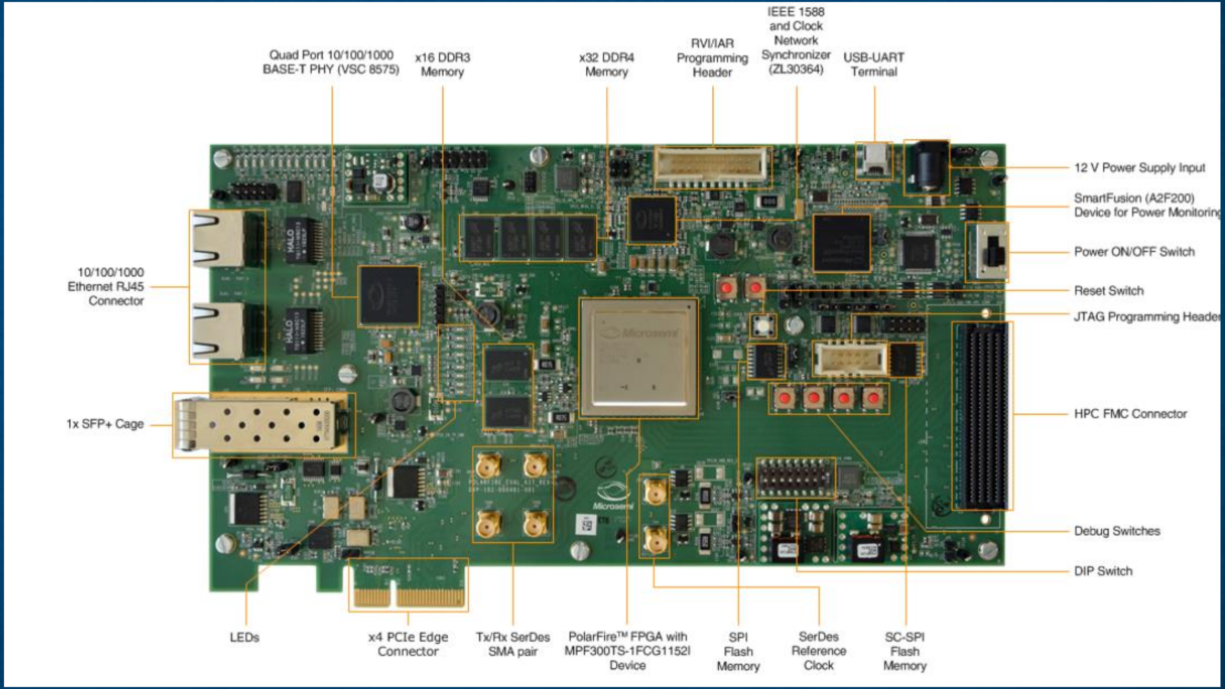
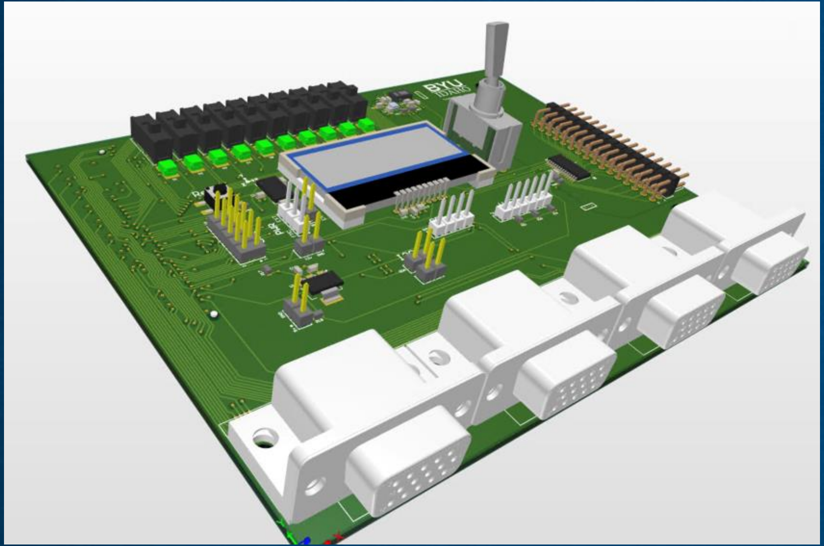
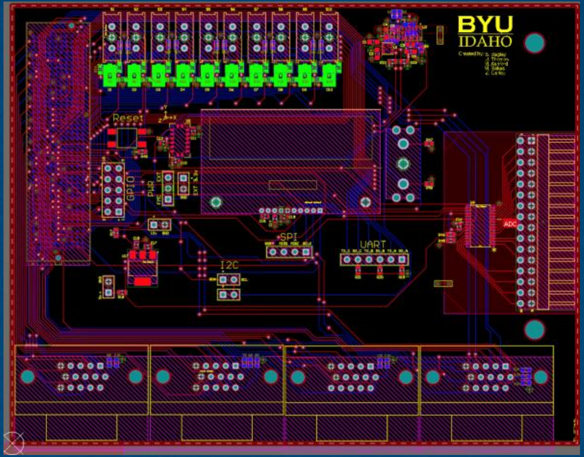
Hardware & Software:

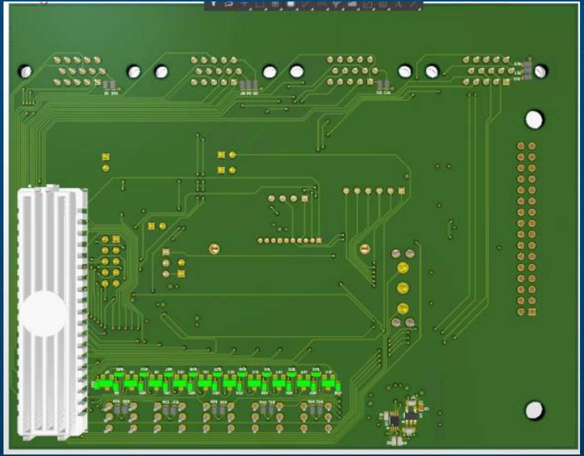
- PolarFire FPGA
- Libero
- SoftConsole
- Altium



PCB Render:







Libero:

integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, Programming & Debug Tools capabilities, and secure production programming support.

Accomplished:

- **Setup Libero by solving problems with computer hardware and software, as well as fixing issues with anti-virus and physical constraints.**
- **Created a base RISC-V processor in TMR**
- **Started initial configuration of 3 other cores**
- **Created the SPI, I2C, UART, and GPIO modules**
- **Started the creation of the LVDS UART**

Yet to be done:

- **Finish the other three processor designs.**
- **Fix memory controller compatibility issues between AHB processors and AXI memory.**
- **Finish the LVDS UART**
- **Fully test SPI, I2C, GPIO, and LVDS UART**

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Problems Overcome:

- **Finding out that the computer needed 16GB of RAM to synthesize**
- **The anti-virus software (Sophos & Windows Defender) automatically deletes the rwnetlist tool.**
- **Finding that the user needs to disable Sophos completely, copy the rwnetlist file from another folder into the needed directory, run that specific file, and tell Windows Defender to run it anyway with admin privileges**
- **Issues with Place&Route not able to map I/O signals correctly**
- **Place&Route can take over an hour due to the low specs of school computers**

Problems Not Overcome:

- **Mapping the LVDS UART I/O signals correctly**
- **Having multiple people work on the project with only 1 license**

SoftConsole: Free software development environment facilitating the rapid development of bare-metal and RTOS based C/C++ software for Microsemi CPU and SoC based FPGAs.

Accomplished:

- Created a SoftConsole project that can run on the first processor design
- Finished basic driver code for the LCD screen and ADC that can possibly run on other core configurations (depending on if the APIs change between processors)
- Finished testing code for SPI, I2C, and CPU. Can possibly run on other core configurations (depending on if the APIs change between processors)
- Created basic benchmarking code

Yet to be done:

- Fully test all of the code (some testing has been done by mapping the FPGA connections to the 6 available header pins on the FPGA)
- Write driver code for all of the sensors
- Write test program for LCD screen, LVDS UART, sensors, ADC, and GPIO

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SoftConsole: **Free software development environment facilitating the rapid development of bare-metal and RTOS based C/C++ software for Microsemi CPU and SoC based FPGAs.**

Problems Overcome:

- **Adding in new driver libraries for new modules such as I2C**
- Correctly configuring the memory addresses for each module so they match with the settings in the Libero project
- Properly building and uploading code to FPGA

Problems Not Overcome:

- **Running code on FPGA in debug mode was very finicky**

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Altium:

PCB design software and high-powered tools for PCB designers. Industry-leading schematic capture, layout and prototyping tools.

Accomplished:

- **Imported and created footprints and CAD models for all PCB components**
- **Designed schematics for all pieces showing how everything connects and interfaces with FMC HPC connector**
- **Created PCB layout by routing all pads to their correct connections**
- **Figured out what FMC HPC connections that will interface with the PolarFIre FPGA**
- **Ordered and received completed PCB and components**

Yet to be done:

- **Place and solder all components using the solder mask, solder paste, and a reflow oven**
- **Use probe to test the connections and inspect solder joints**
- **Test as many connections and routes on the PCB as possible BEFORE plugging it into the FMC to verify that the FPGA will not be damaged in any way**
- **Test everything using the FPGA and SoftConsole. Make sure that the LVDS UART is reliable and the LCD screen and 3 position toggle switch works**

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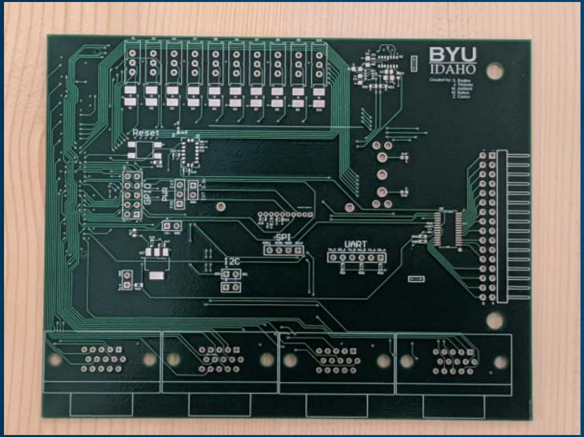

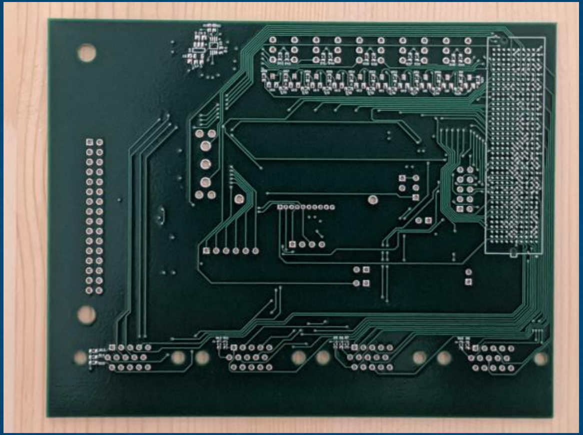

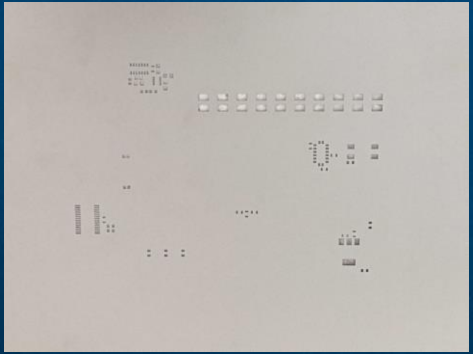

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Problems Overcome:

- **Had issues with the built in version control**
- **Issue ordering the solder masks**

Problems Not Overcome:

- **Differential pairs not spaced far enough from other differential pairs preventing high speed performance**
- **Altium crashes if too many programs are being run**
- **Difficulties with the Signal Integrity option**

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Future Areas of Improvement:

PCB

- **Solder on components**
- **Test functionality**
- **Design a high speed capable board**
- **Space out connections on FMC for ease of routing**

Libero

- **More architectures**
- **Benchmark CPUs**

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Questions?