Week 7 (18-Feb to 23-Feb) Zac Carico

Goal/Task	% Done	Hours (Act.)
Helped Teammates with Altium	N/A	4
Accelerometer Schematic	99.99%	2
Tried to install Libero	1%	5

Hours on task during the week (On track ≥ 10 / wk)	11
Total hours on task so far this semester (On track ≥ 80 hrs)	

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Progress made during the week (Log)

(What I did)

For example: Resources found (links, manuals), Designs created, Decisions made and corresponding rational, Photos of prototype progress, etc.

- Got in contact with Randy about issues with Libero
- Helped teammates with Altium and worked on the top module
- Most of the schematics are complete

Difficulties encountered during the week
(What I did not do and why)

- Libero
- Libero
- Libero
- Finding times when computers are open

Goals for this coming week

(Ones that move the project forward the most)

Goal/Task	Stop Date (Est.)	Hours (Est.)
Get Libero installed	N/A	Indef
Help rest of team complete Schematics and Layout	Next Sun	5hrs
Try to find open source RISC-V cores and implement everything without Libero	N/A	8hrs

Estimated time needed to work on goals for this coming week (typ. 13 hrs)	13hrs

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How can we help you achieve your goals?

- Brother Smith: Can you help us go over our schematics and the PCB layout (when that's finished?)

Week 7 (18-Feb to 23-Feb) James Thomas

Goal/Task	% Done	Hours (Act.)
Schematic – mostly fixing errors	50	7
Playing with PLLs / UART	10	3

Hours on task during the week (On track ≥ 10 / wk)	10
Total hours on task so far this semester (On track ≥ 80 hrs)	70

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Progress made during the week (Log)

(What I did)

Attempted fixing schematic errors.

Started UART implementation (generating the BAUD rate) for Artix-7 only

Difficulties encountered during the week
(What I did not do and why)

- Using Libero – people keep using our computers

Goals for this coming week

(Ones that move the project forward the most)

Goal/Task	Stop Date (Est.)	Hours (Est.)
Layout design / fixing schematic errors		10
UART implementation		3

Estimated time needed to work on goals for this coming week (typ. 13 hrs)	13

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How can we help you achieve your goals?

- Ban people from computers 1-4

Week 7 (18-Feb to 23-Feb) Max Bakes

Goal/Task	% Done	Hours (Act.)
SpI testing	20%	9
ADC harness	-30%	2

Hours on task during the week (On track ≥ 10 / wk)	11
Total hours on task so far this semester (On track ≥ 80 hrs)	74

Progress made during the week (Log)

(What I did)

For example: Resources found (links, manuals), Designs created, Decisions made and corresponding rational, Photos of prototype progress, etc.

Began testing SPI.

Tried to fix ADC harness and apparently deleted it.

Difficulties encountered during the week

(What I did not do and why)

Software issues.

Goals for this coming week

(Ones that move the project forward the most)

Goal/Task	Stop Date (Est.)	Hours (Est.)
Readd ADC	today	1
SPI test	2/26	3
Board layout	2/28	9

Estimated time needed to work on goals for this coming week (typ. 13 hrs)	

How can we help you achieve your goals?

I might need help re-adding the ADC.

Week 7 (18-Feb to 23-Feb) Sam Bagley

Goal/Task	% Done	Hours (Act.)
Schematic Design	%95	12

Hours on task during the week (On track ≥ 10 / wk)	12
Total hours on task so far this semester (On track ≥ 80 hrs)	76

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Progress made during the week (Log)

(What I did)

For example: Resources found (links, manuals), Designs created, Decisions made and corresponding rational, Photos of prototype progress, etc.

- Work a long time on schematics. Added numbers to all components, (even though Altium apparently does that automatically)
- Attempted to create PCB layout but the Compiler had over 300 errors and warnings. I managed to remove the critical warnings, and got the total to under 200, but we need to fix the rest before it will import all parts into the PCB properly.

Difficulties encountered during the week

(What I did not do and why)

Altium gave me many, many errors when trying to add to the PCB design. We've got to fix them all before all the footprints will show up.

Goals for this coming week

(Ones that move the project forward the most)

Goal/Task	Stop Date (Est.)	Hours (Est.)
PCB design	3/1	13

Estimated time needed to work on goals for this coming week (typ. 13 hrs)	13hrs

How can we help you achieve your goals?

Meet together tomorrow morning to fix schematics?

Week 7 (18-Feb to 23-Feb) Michael Ashford

Goal/Task	% Done	Hours (Act.)
Fix Libero	%95	6
Setup Git in Libero	100%	2

Hours on task during the week (On track ≥ 10 / wk)	8
Total hours on task so far this semester (On track ≥ 80 hrs)	56

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Progress made during the week (Log)

(What I did)

Talked to support about problems (haven't gotten a response since Thursday)

Uninstalled Libero, but didn't have admin rights to reinstall.

Researched Git for Libero (there is no baked in support)

Difficulties encountered during the week
(What I did not do and why)

Had to travel home for most of the week to visit grandmother
Microsemi never got back to me when I sent them the project files

Goals for this coming week

(Ones that move the project forward the most)

Goal/Task	Stop Date (Est.)	Hours (Est.)
Create RISC-V in TMR	3/2/20	7
Research RISC-V programs	3/2/20	4
LCD Interface	3/2/20	4

Estimated time needed to work on goals for this coming week (typ. 13 hrs)	13hrs

How can we help you achieve your goals?

Sit down with Zac and attempt a rough draft of TMR with processors
We only have 8 GB of RAM, PolarFire boards require 16GB for synthesis