Proposal

Triple Modular Redundancy Implemented Through RISC-V Architecture on an FPGA

PO# PC11801312

by

BYU-Idaho ECEN 499 W20 and S20 Senior Design Team

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Team members:

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Description:

Create and test a system using Triple Modular Redundancy (TMR) with various configurations of the RISC-V open source instruction set on Microsemi's PolarFire radiation tolerant FPGA. This is to test the possibility of using RISC-V architecture in space, specifically the possibility of implementing this system in the Caution and Warning System (CWS) in the xEMU.

Methodology:

The finished PCB designed by last semesters senior design team will be manually populated and soldered if an SMT assembly company cannot be found.

To implement the TMR RISC-V cores, and program the PolarFire board, Microsemi's IDE will be used to create the VHDL code. There is only one machine licensed for the software, so a network will be established at the home of one team member where that machine can be accessed. This will allow all

members access to the system remotely. This is of course is contingent on whether permission is granted by the school to remove the machine from the lab.

<u>**Hardware:**</u>

- PolarFire FPGA by Microsemi
- LCD Screen
- Radiation Sensor (Geiger Counter)
- Heartrate Monitor
- Pressure Sensor
- Temperature/Humidity Sensor
- Custom PCB with headers for GPIO, SPI, I2C, and UART. Ordered from China
- LEDs, switches, buzzers

Our custom PCB will house the LCD, the various sensors and components in use, and the connector that will attach onto the FPGA. We wanted to focus on monitoring astronaut vitals while in their suits. The heartrate monitor will look out for any elevations that could indicate problems. The temperature and humidity sensor will be used for temperature control in the suit. The pressure sensor will look out for suit leaks. The radiation sensor will monitor outside conditions and alert the astronaut to critical amounts of radiation. LEDs and buzzers will supplement the LCD screen in alerting the astronaut to danger.

<u>**Deliverables:**</u>

First deliverable will be this proposal. Afterwards, there will be a weekly status update on the project. At the end of the project, there will be the source code and documentation for the project, report on all research and testing done, JSC Form 290, completed PCB, and the PolarFire FPGA flashed with the final system design.